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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/645,646	08/22/2003	Guy Moshe Cohen	YOR920030328US1	8783
21254	7590	03/16/2006		EXAMINER
MCGINN INTELLECTUAL PROPERTY LAW GROUP, PLLC 8321 OLD COURTHOUSE ROAD SUITE 200 VIENNA, VA 22182-3817			BLUM, DAVID S	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 03/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/645,646	COHEN, GUY MOSHE	
	Examiner	Art Unit	
	David S. Blum	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 08 November 2005.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-12,21-24 and 28-33 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-12,21-24 and 28-33 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

✓

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ . |

This action is in response to the election filed 4/20/05.

DETAILED ACTION

Claim Objections

1. Claim 29 is objected to because of the following informalities: Claim 29 recites "separated from the gater". It is believed "gater" should be "gate". Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-12, 21-24, and 28-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Joshi (US006921982B2).

Joshi teaches the device of claims 1-12, 21-24, and 28-33 as follows.

Regarding claim 1, Joshi teaches a channel of strained silicon germanium adjacent a source and drain (12 and 14), column 10 lines 9-10), two gates (88 and 89), the gates

on a dielectric layer (see column 6 lines 13-18, gate on dielectric), and the channel is non-planar (figure 8F).

Regarding claim 2, the channel thickness is relatively uniform (figure 8F).

Regarding claim 3, the channel material may be epitaxially grown (column 8 lines 1-4).

Regarding claim 4, Joshi forms high quality SiGe free from dislocations (column 7 lines 18-20). The examiner considers this to mean "defect free".

Regarding claim 5, the strained-silicon channel includes a distorted lattice cell. This is inherent to a strained layer.

Regarding claim 6, the gates are independently controlled (column 10 line 12).

Regarding claim 7, the strained silicon channel comprises a fin (figure 8F and column 10 line 4).

Regarding claim 8, the first and second gates are self-aligned (islands are precision aligned (column 7 lines 39-40), thus resulting gates would be self aligned.).

Regarding claim 9, the limitation of forming the first and second gates in a single lithography step is a process limitation (product by process) and has no patentable weight in device claims.

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patentability of a product does not depend on its method of production." MPEP 2113

Regarding claim 10, the first and second gates are self-aligned as above (see claim 8) and also aligned with the source and drain, thus all are self-aligned.

Regarding claim 11, the background of the invention teaches that it is known to use one or more fins (column 1 line 42-44). Also see column 7 lines 64-65 and column 8 lines 42-43).

Regarding claim 12, the device includes a planarized top (figure 8F).

Regarding claim 28, the first gate is separated from the second gate (figure 8F).

Regarding claim 32, the claim is a product by process claim and the process is given no patentable weight.

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patentability of a product does not depend on its method of production." MPEP 2113

Regarding claim 21, Joshi teaches a channel of strained silicon germanium adjacent a source and drain (12 and 14), column 10 lines 9-10), two gates (88 and 89), the gates on a dielectric layer (see column 6 lines 13-18, gate on dielectric), and the channel is non-planar (figure 8F), the strained silicon channel comprises a fin (figure 8F and column 10 line 4).

Regarding claim 22, a circuit may comprise the device of claim 1 (column 1 lines 14-45).

Regarding claim 23, the strained silicon channel is compressively strained (column 5 line 45).

Regarding claim 24, the strained silicon channel is compressively strained (column 5 line 45 and column 6 line 66).

Regarding claim 29, the first gate is separated from the second gate (figure 8F).

Regarding claim 33, the claim is a product by process claim and the process is given no patentable weight.

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patentability of a product does not depend on its method of production." MPEP 2113

Regarding claim 30, Joshi teaches a channel of strained silicon germanium adjacent a source and drain (12 and 14), column 10 lines 9-10), two gates (88 and 89), the gates on a dielectric layer (see column 6 lines 13-18, gate on dielectric), and the channel is non-planar (figure 8F), and the first and second sidewalls are opposing to each other (figure 8F).

Regarding claim 31, Joshi teaches a channel of strained silicon germanium adjacent a source and drain (12 and 14), column 10 lines 9-10), two gates (88 and 89), the gates on a dielectric layer (see column 6 lines 13-18, gate on dielectric), and the channel is non-planar (figure 8F) and is fixed to the substrate by the first and second gates (figure 8F).

Response to Arguments

4. Applicant's arguments filed 11/8/05 have been fully considered but they are not persuasive.

The applicant argues that Joshi does not teach the combination of claim 1 or 21..

The examiner disagrees.

The applicant argues that Joshi is different from the claimed invention. The examiner disagrees as Joshi reads on the current claims.

The applicant argues that the fins of Joshi are too thick and therefore Joshi does not form a FINFET but rather two FETs in parallel. The applicant notes that Joshi reads on the claims, refers to the strained channel as a fin, and the claims do not limit the invention to a FINFET (claims 7, 11, 21, 29, 33 do require the strained channel to comprise a fin). The other claims do not require such a limitation.

The applicant argues that Joshi does not form a FINFET as defined by HU. However, the device of Joshi does read on the present claims and Joshi refers to the device as a FINFET.

The applicant argues that the core material is not a gate. The examiner never made such a representation.

The applicant argues that Joshi does not form a double-gate FINFET as there is no second gate on the inner sidewall to control the channel. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., double-gate FINFET as there is

no second gate on the inner sidewall to control the channel) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Joshi forms a second gate on an opposing wall as required by the claims.

The applicant argues that Joshi has SiGe in contact with Si and this is undesirable. As above, there are no limitations in the claims for the basis of such an argument.

The applicant argues that Joshi does claim that the SiGe is free from dislocation, but to the inventor's knowledge, experimental data does not support this claim. However, the patent, by law, is considered enabled. Arguments are not considered in this matter. Conclusive proof would be necessary to show that the claim of Joshi is not enabled.

The applicant argues that Joshi does not teach how to obtain the above benefit, only that it is present. However, the claims at hand are device claims, and absent evidence to the contrary, Joshi is considered to have the benefits disclosed.

The applicant again argues that Joshi does not form a FINFET but two FETs in parallel. However, Joshi reads on the present claims and refers to the device as a FINFET.

The applicant argues that while Joshi teaches that the islands are precision aligned, they are not aligned to the source and drain. Claim 8 only requires the gates be self aligned, and claim 10 that the gates source and drain are self aligned with respect to each other. As the islands are precision aligned, the gates are aligned with respect to the source and drain. The applicant argues that Joshi does not teach how to self align the gates to the source and drain. The method is immaterial in a device claim. The gates only need be aligned (in any fashion) to the source/drains.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Blum whose telephone number is (571)-272-1687) and e-mail address is David.blum@USPTO.gov .

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr., can be reached at (571)-272-1702. Our facsimile number all patent correspondence to be entered into an application is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



David S. Blum

March 14, 2006